

Claims

What is claimed is:

- 1 1. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation comprising:
3 a plurality of field effect transistors (FETs); said plurality of FETs
4 defining a storage cell and a pair of wordline FETs coupled to said storage
5 cell; each of said plurality of FETs having a device structure extending in a
6 single direction;
7 said device structure of each of said plurality of FETs including a
8 diffusion layer, a polysilicon layer and first metal layer;
9 a local interconnect connecting said diffusion layer, said polysilicon
10 layer and said first metal layer;
11 each of said pair of wordline FETs having a gate input connected to a
12 wordline; said wordline including a single wordline for implementing one-port
13 operation or two separate wordline connections for implementing two-port
14 operation.
- 1 2. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 1 wherein
3 each of said plurality of FETs having said device structure extending in said
4 single direction include each of said plurality of FETs having a width
5 extending in a first direction and length extending in a second direction; said
6 first and second directions being offset by 90°.
- 1 3. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 1 wherein
3 said plurality of FETs include a plurality of both N-channel field effect
4 transistors (NFETs) and P-channel field effect transistors (PFETs).
- 1 4. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 3 wherein
3 said storage cell includes a pair of inverters, each inverter formed by one
4 PFET and one NFET connected between voltage supply rail and ground
5 connections and having a common gate connection of said one PFET and
6 one NFET connected to an output of said other one of said pair of inverters.

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1 5. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 4 wherein
3 said voltage supply rail and ground connections includes said first metal
4 layer.

1 6. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 4 wherein
3 said common gate connection of said one PFET and one NFET includes
4 said polysilicon layer.

1 7. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 1 wherein
3 said local interconnect includes a metal local interconnect disposed on said
4 diffusion and polysilicon layers for electrically connecting said diffusion and
5 polysilicon layers and a metal contact extending between said metal local
6 interconnect and said first level metal for electrically connecting said
7 diffusion and polysilicon layers and said first level metal.

1 8. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 1 wherein
3 said local interconnect includes a metal contact disposed on said diffusion
4 and polysilicon layers and extending to said first level metal for electrically
5 connecting said diffusion and polysilicon layers and said first level metal.

1 9. A compact static random access memory (SRAM) cell layout
2 for implementing one-port or two-port operation as recited in claim 1 wherein
3 said local interconnect includes a conduction layer disposed on a butted
4 diffusion connection of diffusion-p type and diffusion-n type and a metal local
5 interconnect disposed on said conduction layer.

10. A compact static random access memory (SRAM) cell layout for implementing one-port operation comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer;

each of said pair of wordline FETs having a gate input connected to a single wordline for implementing one-port operation.

11. A compact static random access memory (SRAM) cell layout for implementing one-port operation as recited in claim 10 wherein each of said plurality of FETs having said device structure extending in said single direction include a plurality of both N-channel field effect transistors (NFETs) and P-channel field effect transistors (PFETs) and each of said plurality of NFETs and PFETs having a width extending in a first direction and length extending in a second direction; said first and second directions being offset by 90°.

12. A compact static random access memory (SRAM) cell layout for implementing one-port operation as recited in claim 11 wherein said storage cell includes a pair of inverters, each inverter formed by one PFET and one NFET connected between voltage supply rail and ground connections and having a common gate connection of said one PFET and one NFET connected to an output of said other one of said pair of inverters.

13. A compact static random access memory (SRAM) cell layout for implementing one-port operation as recited in claim 10 wherein said local interconnect includes a metal local interconnect disposed on said diffusion and polysilicon layers for electrically connecting said diffusion and polysilicon layers and a metal contact extending between said metal local interconnect and said first level metal for electrically connecting said diffusion and polysilicon layers and said first level metal.

1 14. A compact static random access memory (SRAM) cell layout
2 for implementing one-port operation as recited in claim 10 wherein said local
3 interconnect includes a metal contact disposed on said diffusion and
4 polysilicon layers and extending to said first level metal for electrically
5 connecting said diffusion and polysilicon layers and said first level metal.

1 15. A compact static random access memory (SRAM) cell layout
2 for implementing two-port operation comprising:

3 a plurality of field effect transistors (FETs); said plurality of FETs
4 defining a storage cell and a pair of wordline FETs coupled to said storage
5 cell; each of said plurality of FETs having a device structure extending in a
6 single direction;

7 said device structure of each of said plurality of FETs including a
8 diffusion layer, a polysilicon layer and first metal layer;

9 a local interconnect connecting said diffusion layer, said polysilicon
10 layer and said first metal layer;

11 each of said pair of wordline FETs having a gate input connected to a
12 respective wordline of two separate wordline connections for implementing
13 two-port operation.

1 16. A compact static random access memory (SRAM) cell layout
2 for implementing two-port operation as recited in claim 15 wherein said local
3 interconnect includes a metal local interconnect disposed on said diffusion
4 and polysilicon layers for electrically connecting said diffusion and polysilicon
5 layers and a metal contact extending between said metal local interconnect
6 and said first level metal for electrically connecting said diffusion and
7 polysilicon layers and said first level metal.

1 17. A compact static random access memory (SRAM) cell layout
2 for implementing two-port operation as recited in claim 15 wherein said local
3 interconnect includes a metal contact disposed on said diffusion and
4 polysilicon layers and extending to said first level metal for electrically
5 connecting said diffusion and polysilicon layers and said first level metal.

1 18. A compact static random access memory (SRAM) cell layout
2 for implementing two-port operation as recited in claim 15 wherein each of
3 said plurality of FETs having said device structure extending in said single
4 direction include a plurality of both N-channel field effect transistors (NFETs)
5 and P-channel field effect transistors (PFETs) and each of said plurality of
6 NFETs and PFETs having a width extending in a first direction and length
7 extending in a second direction; said first and second directions being offset
8 by 90°.

1 19. A compact static random access memory (SRAM) cell layout
2 for implementing two-port operation as recited in claim 18 wherein said
3 storage cell includes a pair of inverters, each inverter formed by one PFET
4 and one NFET connected between voltage supply rail and ground
5 connections and having a common gate connection of said one PFET and
6 one NFET connected to an output of said other one of said pair of inverters.

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